## What is Claimed is:

[c1] A writeback and refresh circuit for a direct sense architecture memory comprising:

a global data line;

a plurality of primary sense amps connected to the global data line and also connected to bitlines, each of which is coupled to an array of memory storage cells which are selected for write and read operations by a plurality of wordlines;

a single secondary sense amp connected to the global data line, wherein the secondary sense amp receives data from the primary sense amps over the global data line, and includes a restore/writeback circuit to writeback data over the global data line to a primary sense amp and back into the memory.

[c2] The circuit of claim 1, wherein the secondary sense amp includes a latch.

[c3] The circuit of claim 1, wherein each primary sense amp includes at least one direct sense device, and only the gate of each direct sense device is connected to a bitline, such that the direct sense device does not provide any feedback to or alter the signal on the bitline.

[c4] The circuit of claim 1, wherein each primary sense amp includes:

a precharge/equalize device, coupled between a power supply and a bitline;

a write device, coupled between the global data line, and the bitline;

a read device, coupled between the bitline and the global data line;

a read enable/switch device, coupled in series with the read device and ground.

[c5] The circuit of claim 1, wherein each primary sense amp includes:

a pair of precharge/equalize devices, coupled between a power supply and a pair of bitlines;

a pair of write switch devices, coupled between the global data line and the pair of respective bitlines;

a pair of read devices, coupled between the pair of respective bitlines and

the global data line;

a pair of read enable switch devices, coupled in series with the pair of respective read devices and ground.

[c6] The circuit of claim 1, wherein the secondary sense amp comprises:

a current supply device, connected between a power supply and the global data line;

a resistive isolation device, biased to operate in its linear range of operation, coupled between the global data line and a cross couple inverting latch which isolates/decouples the global data line from the cross couple inverting latch;

a cross couple inverting latch, coupled to the output of the resistive isolation device, including a pair of latch devices and a pair of feedback devices which provide a weak feedback signal such that the latch is stable in a first state but is more stable in a second state, such that it is more easily switched from the first state to the second state than vice versa, to provide a hair trigger type of switching operation;

a pair of invertors, coupled between the output of the latch and an output node, to provide buffering therebetween and also to convert the latch output signal to a signal at ground for a data 0 and at full rail voltage for a data 1;

a pull down and inverting device connected between the output node and a data out line;

a refresh/rewrite device, connected between the output node and the global data line, which is turned on during a refresh/rewrite operation to rewrite data back into the memory;

a data write device, connected between a data in line and the global data line, which is turned on during a data write operation to write data into the memory.

[c7] The circuit of claim 6, further including

a current enable/switch device connected in series with the current supply device between the power supply and the global data line;

a precharge device, coupled between the power supply and the input to

the latch.

[c8] The circuit of claim 7, wherein during a 2-cycle memory read and refresh operation, in a first memory read cycle data is transferred from one array in the memory through a primary sense amp to the secondary sense amp which is multiplexed and shared between the plurality of primary sense amps, and in a second memory refresh cycle data is transferred from the secondary sense amp to a selected primary sense amp back to the one array in the memory.

[c9] The circuit of claim 8, wherein during the second memory refresh cycle in the secondary sense amp, the current enable/switch device and the resistive isolation device are turned off, and then the refresh device is turned on with a boosted gate signal, and in the primary sense amp, a write device is turned on.

[c10] The circuit of claim 9, wherein during the 2 cycle memory write refresh operation, the wordline remains active for 2-cycles with no interim reset.

[c11] The circuit of claim 10, wherein in the first cycle a primary sense amp senses the data on a bitline, and transfers the data over the global data line as an analog level signal to a latch in the multiplexed secondary sense amp which digitizes the data, and in the second cycle the digitized data is returned over the global data line as a full-rail digital signal back to the primary sense amp which writes the data back into the memory array.

[c12] The circuit of claim 11, wherein in the secondary sense amp the analog data is converted to digital data by the resistive isolation device and the cross couple inverting latch, after which the resistive isolation device and the current supply device are shut off, after which the writeback back device is enabled to pass the inverted and amplified data back to the memory array cell over the global data line.

[c13] The circuit of claim 1, wherein during a 2-cycle memory read and refresh operation, in a first memory read cycle data is transferred from one array in the memory through a primary sense amp to the secondary sense amp which is multiplexed and shared between the plurality of primary sense amps, and in a second memory refresh cycle data is transferred from the secondary sense amp

to a selected primary sense amp back to the one array in the memory.

[c14] The circuit of claim 13, wherein during the 2 cycle memory write refresh operation, the wordline remains active for 2-cycles with no interim reset.

[c15] The circuit of claim 14, wherein in the first cycle a primary sense amp senses the data on a bitline, and transfers the data over the global data line as an analog level signal to a latch in the multiplexed secondary sense amp which digitizes the data, and in the second cycle the digitized data is returned over the global data line as a full-rail digital signal back to the primary sense amp which writes the data back into the memory array.

[c16] The circuit of claim 1, wherein in the first cycle a primary sense amp senses the data on a bitline, and transfers the data over the global data line as an analog level signal to a latch in the multiplexed secondary sense amp which digitizes the data, and in the second cycle the digitized data is returned over the global data line as a full-rail digital signal back to the primary sense amp which writes the data back into the memory array.

[c17] A primary sense amp comprising:

a precharge/equalize device, coupled between a power supply and a bitline;

a write device, coupled between the global data line, and the bitline;

a read device, coupled between the bitline and the global data line;

a read enable/switch device, coupled in series with the read device and ground;

an inverter coupled between the global data line and the write device, such that inverted digitized data on the global data line is inverted and directed through the write device.

[c18] The circuit of claim 17, wherein the power supply for the inverter is switched off during a read operation, and powered on during a write operation.

[c19] A primary sense amp comprising:

a pair of precharge/equalize devices, coupled between a power supply and a pair of respective bitlines;

a pair of write devices, coupled between the global data line and the pair of respective bitlines;

a pair of read devices, coupled between the pair of respective bitlines and the global data line;

a pair of read enable switch devices, coupled in series with the pair of respective read devices and ground;

a pair of inverters, coupled between the global data line and the pair of respective write devices.

[c20] The circuit of claim 19, wherein the power supply for the inverter is switched off during a read operation, and powered on during a write operation.